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Title: SEMICONDUCTOR DEVICE INCLUDING PROTECTION MEANS ;

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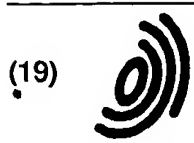
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**ABSTRACT:**

An ESD protection circuit (100) and method is described herein. A lateral npn transistor (104) is connected between an I/O pad (110) and ground (GND). A substrate biasing circuit (150) increases the voltage across a substrate resistance (114) during an ESD event by conducting current through the substrate. This, in turn, triggers the lateral npn (104) which clamps to voltage at the pad (110) and dissipated the ESD current. The lateral npn (104) is the primary protection device for dissipating ESD current.



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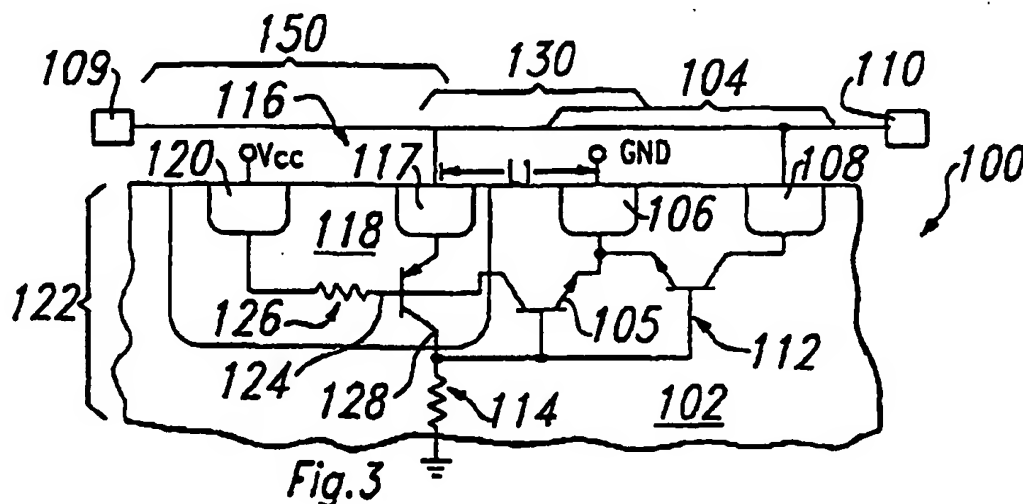
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(54) **Semiconductor device including protection means**

(57) An ESD protection circuit (100) and method is described herein. A lateral npn transistor (104) is connected between an I/O pad (110) and ground (GND). A substrate biasing circuit (150) increases the voltage across a substrate resistance (114) during an ESD event by conducting current through the substrate. This,

in turn, triggers the lateral npn (104) which clamps to voltage at the pad (110) and dissipates the ESD current. The lateral npn (104) is the primary protection device for dissipating ESD current.



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## Description

### FIELD OF THE INVENTION

This invention generally relates to semiconductor devices and processes and more specifically to ESD protection in CMOS integrated circuits.

### BACKGROUND OF THE INVENTION

As integrated circuits (ICs) become more complex and more dense, the nominal supply voltage drops. Whereas, once nominal supply voltages were in the 5V range and then the 3.3V range, state of the art ICs today have a nominal supply voltage of approximately 2.5 V. However, these ICs must operate in systems designed for older ICs having a 3.3V nominal supply voltage. Thus, today's ICs are expected to be able to sustain 3.3 V at the input/output (I/O) pins without excessive leakage or any permanent damage occurring. However, since a gate oxide of the order of 60 Å is used in the newer ICs, there is a possibility of reliability problems related to gate oxide wear-out based on time dependent dielectric breakdown analysis. In addition, the ICs are expected to be power-up sequence independent. That is, when the supply voltage is at 0 V, the IC needs to be able to tolerate 3.6 volts at the I/O pins without permanent damage or excessive oxide stressing.

These requirements place major restrictions on the electrostatic discharge (ESD) protection circuit design. Gate oxides cannot be connected directly between the I/O pads and ground. Thus, typical ESD protection circuits such as the gate-coupled nMOS transistor, low voltage triggered SCRs (silicon-controlled rectifiers) and gate-coupled SCRs cannot be used as they have been in the past. One prior art technique that avoids connecting a gate oxide directly between the internal circuitry at the I/O pins and ground in a modified lateral SCR (MLSCR), is shown in Figure 1. The MLSCR 12 is connected between the I/O pin 14 and ground GND. Unfortunately, the trigger voltage of the MLSCR (about 20V) is higher than the breakdown of a gated-diode junction (typically between 8V and 10V) or a gate oxide (typically about 12V - 15V). Hence, a series resistor R is required to enable the voltage at the anode of the MLSCR 12 to reach the SCR trigger level before the internal circuitry 16 is damaged.

Another ESD protection circuit that avoids connecting a gate-oxide directly between the internal circuitry at the I/O pins and ground is a dual-diode circuit, shown in Figure 2. A first diode 20 is connected between the I/O pin 14 and the supply voltage, Vcc and a second diode 22 is connected between I/O pin 14 and ground, GND. However, this circuit has limitations in submicron devices. The voltage-clamping properties of a reversed biased n+/p diode is one limitation. The on-resistance of a reversed-biased diode in avalanche breakdown is greater than 25 ohms. This limits the capability of high current clamping. Accordingly, there is a need for an

improved ESD protection circuit that avoids connecting a gate oxide between internal circuitry and ground.

### SUMMARY OF THE INVENTION

An ESD protection circuit and method for integrated circuits is described herein. A lateral npn transistor is connected between an I/O pad and ground. A substrate biasing circuit is provided that causes current to be conducted through the substrate resistance during an ESD event. This, in turn, raises the voltage across the substrate resistance and forward-biases the emitter-base junction of the lateral npn thus triggering the lateral npn. The lateral npn is the primary protection device for dissipating ESD current.

An advantage of the invention is providing improved ESD protection for multi-voltage applications in submicron, thin oxide CMOS processes.

A further advantage of the invention is providing improved ESD protection for multi-voltage applications that is independent of the power-up sequence in submicron, thin oxide CMOS processes.

A further advantage of the invention is providing improved ESD protection requiring less area in submicron, thin oxide CMOS processes.

These and other advantages will be apparent to those skilled in the art having reference to the specification in conjunction with the drawings.

### BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will now be further described by way of example, with reference to the accompanying drawings in which;

FIG. 1 is a schematic diagram of a prior art ESD protection circuit;

FIG. 2 is a schematic diagram of a prior art dual-diode ESD protection circuit;

FIG. 3 is a partially cross-section/partially schematic diagram of an ESD protection device according to one embodiment of the invention;

FIG. 4 is a partially cross-section/partially schematic diagram of an ESD protection device according to the invention having a diode string;

FIG. 5 is a schematic diagram of an ESD protection device according to the invention including a Darlington circuit;

FIG. 6 is a graph of applied voltage versus number of diodes for various vertical pnp transistor gains;

FIG. 7 is a schematic diagram of an ESD protection device according to the invention including a snubber circuit for reducing reverse leakage current;

FIG. 8 is a schematic diagram of an ESD protection device according to the invention including emitter base resistors in a Darlington circuit for increasing the maximum clamp voltage and reducing the reverse leakage current;

FIG. 9 is a schematic diagram of an ESD protection device according to the invention illustrating a Darlington circuit and multiple lateral npn transistors;

FIG. 10 is a exemplary layout diagram of an ESD protection device according to the invention;

FIG. 11 is a preferred layout of an ESD protection device according to the invention;

FIG. 12 is a schematic diagram of a first alternative embodiment of the invention; and

FIG. 13 is a schematic diagram of a second alternative embodiment of the invention.

Corresponding numerals and symbols in the different figures refer to corresponding parts unless otherwise indicated.

#### DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

An ESD protection device 100 according to the invention is shown in Figure 3. A lateral npn transistor 104 is located in a substrate layer 102. Substrate layer 102 may, for example, comprise a p-type epitaxial layer on a p+ substrate. Lateral npn 104 comprises two n-type diffused regions 106, 108 as the emitter and collector respectively. Diffused regions 106 and 108 are preferably separated by the minimum spacing allowed by design rules, for example of the order of 0.7 microns. Diffused region 106 (the emitter) is connected to ground and diffused region 108 (the collector) is connected to the I/O pad 110. The base 112 is connected to ground through the substrate 102 and its associated resistance 114.

Substrate biasing circuit 150 can be any one of a number of circuits that raises the voltage across the substrate resistance 114 during an ESD event. This, accordingly, raises the voltage at the base of lateral npn 104 to forward bias the emitter-base junction and trigger the npn transistor 104. The npn transistor 104 clamps the voltage at the pad 110 to a voltage of the order of 5-7 volts and dissipates the ESD current. Thus, the internal circuitry 109 is protected.

Substrate biasing circuit 150, in the embodiment shown in Figure 3, comprises a diode 116. Diode 116 comprises a p-type diffused region 117 within n-well 118. P-type diffused region 117 is connected to the I/O pad 110. The supply voltage Vcc is connected to n-well 118 through n-type diffused region 120. Diode 116 thus comprises an inherent vertical pnp transistor 122. Verti-

cal pnp transistor 122 is not a discrete element but is automatically built-in to diode 116 within n-well 118. P-type diffused region 117 forms the emitter of the inherent vertical pnp transistor 122 and the base 124 is connected to the supply voltage Vcc through the n-well 118 resistance 126 and n-type diffused region 120. The collector 128 is connected through the substrate resistance 114 to ground, GND. An advantage of the invention is that it is applicable to CMOS processes without additional masking steps. Alternative substrate biasing circuits will be apparent to those skilled in the art having reference to the specification.

Operation of the above described circuit under ESD conditions will now be described. At a first stage of operation, the voltage at I/O pad 110 reaches the turn-on voltage of vertical pnp 122. This may be on the order of 0.8 V. ESD current then begins to conduct through vertical pnp transistor 122. This raises the voltage across the substrate resistance 114 and accordingly at the base of lateral npn transistor 104. In the second stage of operation, the voltage at the base of lateral npn transistor 104 eventually rises enough to forward bias the emitter-base junction, triggering the npn transistor 104. The clamping voltage of the lateral npn transistor 104 is the same as the snapback voltage of a lateral field oxide MOS device (i.e., of the order of 5-7 V). At this point, the majority of the current dissipates through lateral npn transistor 104. In the last stage of operation, an inherent SCR 130 created by n-type diffused region 106, the substrate 102, the n-well 118 and p-type diffused region 117 triggers providing a second voltage clamp. The spacing L1 between the anode (p-type diffused region 117) and cathode (n-type diffused region 106) of the SCR 130 determines the holding voltage of the SCR 130. This is preferably greater than the burn-in voltage and for accelerated reliability testing of about 4V in an advanced CMOS process. The burn-in voltage may for example be of the order of 4.5V. The SCR 130 is also triggered by the vertical pnp transistor action. The collector current through the p-substrate 102 enables the cathode (n-type diffused region 106) to substrate 102 junction to forward bias triggering an inherent lateral npn transistor 105 and then the inherent SCR 130. The SCR 130 is preferably designed so that once the SCR 130 triggers, the voltage clamps to greater than 4V.

Because the ESD protection device 100 according to the invention does not comprise a thin gate oxide, there are no gate oxide integrity problems associated with multi-voltage operation. Multi-voltage operation occurs when the voltage at the I/O pad 110 can be higher than the designed for supply voltage Vcc. For example, the device is fabricated for 2.5V operation but in operation receives I/O signals ranging from 0 to 3.3 V. Receiving a higher voltage at the I/O pad 110 than the supply voltage Vcc (i.e., 3.3V for a 2.5 V device) does not stress the protection device 100. Furthermore, the ESD protection device 100 is independent of power-up sequence. That is, the device 100 is not stressed when a high signal (i.e., 3.3V) is applied at the I/O pad 110

while the supply voltage  $V_{cc}$  remains at 0V.

In the preferred embodiment of the invention, diode 116 actually comprises a diode string 132 as shown in Figure 4 in order to increase the clamping voltage at the pad for input voltages greater than  $V_{cc}$ . Diode string 132 is connected between the I/O pad 110 and the supply voltage,  $V_{cc}$ . The pn diodes 134 are lateral elements in that the dominant current flow is lateral. However, as shown in Figure 5 and described above, the lateral pn diode actually forms the emitter-base junction of a vertical pnp transistor 122 with the p-type substrate 102 serving as the collector. This creates a multi-stage pnp Darlington circuit 142 as shown in Figure 5. Figure 5 illustrates a four-stage pnp Darlington circuit 142 having four inherent vertical pnp transistors T1-T4. The emitter of the Darlington circuit 142 is connected to the I/O pad 110, the collector is the substrate 102, and the base is connected to the supply voltage  $V_{cc}$ .

The equation governing the total voltage,  $V_{IN}$  across the Darlington circuit is easily determined by considering the gain,  $\beta$  and the forward voltage drop,  $V_D$ , across the base-emitter junction of each pnp transistor as indicated in Figure 5.

The current,  $I_1$ , in the first transistor, T1, is given by,

$$I_1 = I_0 \exp \left( \frac{qV_{D1}}{kT} \right)$$

$I_0$  is the saturation current across the  $p^+/n$  junction and  $V_{D1}$  is the voltage drop across the base-emitter junction. Similarly the current,  $I_2$ , in the second transistor, T2, is given by,

$$I_2 = I_0 \exp \left( \frac{qV_{D2}}{kT} \right)$$

For  $\Delta V = (V_{D1} - V_{D2})$ ,

$$\frac{I_1}{I_2} = \exp \left( \frac{q\Delta V}{kT} \right)$$

or,

$$\Delta V = \frac{kT}{q} \ln \left( \frac{I_1}{I_2} \right)$$

$$\Delta v = \frac{kT}{q} \ln (1+\beta),$$

since  $I_1 = (1+\beta)I_2$ . Hence, it can be shown that for a string of  $n$  transistors,

$$V_{IN} = nV_{D1} - \frac{n(n-1)}{2} \frac{kT}{q} \ln(1+\beta).$$

This equation is valid for  $n \leq V_A/[kT \ln(I_1/I_0)]$ , that is for  $V_{D1} = V_A/n$ . It must be noted that it is assumed that  $\beta$  is independent of current in this equation for simplified analysis.

The equation indicates that because of the gain,  $\beta$ , of the vertical pnp, the voltage drop will not be equal across each diode, and beyond a certain  $n$  there will no longer be any diode current. The maximum number of diodes that can successfully be used in series is determined by the gain,  $\beta$ , of the pnp. Assuming  $V_{D1} = 0.6V$ , a plot of the maximum  $V_A$  as a function of the number of diodes is shown in Figure 6 for  $\beta$  of 5, 10 and 20. For a gain,  $\beta$ , of 10, the maximum voltage clamp for a straight diode string is  $\approx 3.3V$ , and for a  $\beta$  of 5, a 4V clamp is achieved with an 11 diode string. The maximum  $V_A$  occurs for strings of  $> 12$  diodes.

It should be noted that in a high gain process, the emitter areas of the different stages need not be the same. Since the current decreases in the stages closer to  $V_A$  these transistors can have proportionately smaller areas.

If desired, a snubber circuit may be used to reduce the reverse leakage current between  $V_{cc}$  and the pad in normal operation. For example, a snubber transistor 144 may be placed between the base of the first stage of the Darlington circuit 142 and the base of the final stage as shown in Figure 7. The purpose of the snubber transistor 144 is to clamp the voltage at the base of the first stage to that of one forward biased diode below the supply voltage  $V_{cc}$ . This snubs the other pnp stages until the voltage at the I/O pad 110 exceeds the supply voltage,  $V_{cc}$ .

Optional feed-forward resistors R1-R3 may be placed between the different diodes of the Darlington circuit 142 as shown in Figure 8 to increase the clamping voltage onto the pad and reduce the reverse leakage current. Resistors R1-R3 increase the clamping voltage by ensuring that transistors closer to  $V_{cc}$  are turned on. In addition, without resistors R1-R3, the first stages of the Darlington circuit 142 carry most of the current and the later stages may not turn on. Resistors R1-R3 allow current to flow in parallel with each of the Darlington stages and control the voltage drop across each stage. For an equal voltage drop across each stage, the resistors are proportioned as  $R, R/2, R/3, \dots, R/(n-1)$  for  $n$  stages. For example, for a 1 mA current limit at the I/O pad 110 and a 6 diode string with a resistor across every two diodes,  $R$  is  $2k\Omega$ .

As shown in Figure 9, lateral npn transistor 104 can also comprise a plurality of lateral npn transistors transistor N1-N4. The base of each lateral npn N1-N4 is connected to the substrate resistance 114. Each emitter is connected to ground ( $V_{ss}$ ) and each collector is connected to I/O pad 110.

An exemplary layout for the invention is shown in Figure 10. The layout of Figure 10 assumes a four stage Darlington circuit. However, those skilled in the art will realize that the number of stages may vary. The lateral npn transistors N1-N4 are formed using n-type diffused

a) regions 106,108 within substrate 102. The n-type diffused regions 106 and 108 alternate between connecting to ground Vss (n-type diffused regions 106) and the I/O pad 110 (n-type diffused regions 108). The spacing L2 between diffused regions 106 and 108 is preferably the minimum allowed by the design rules (i.e., of the order of 0.7 microns). Each diffusion width, D1 and D2 is of the order of 3 microns.

The diodes 134/pnp transistors T1-T4 are each formed in a separate well regions 118 using one p-type diffused region 117 and one n-type diffused region 120 in each well region 118. The p-region 117 of the first pnp transistor stage T1 is connected to the I/O pad 110. The n-region 120 is connected to the p-region 117 of the second stage T2. The n-region 120 of the second stage T2 is then connected to the p-region 117 of the third stage T3 and so on until the last stage T4. The n-region 120 of the last stage T4 is connected to the supply voltage Vcc. The n-well to n-well spacing may be the minimum allowed to conserve area, for example 3 microns. The p- and n- diffused region widths D3 may be of the order of 5 microns and the spacing L1 between the p-type diffused region 117 of the first stage and the nearest n-type diffused region 106 may be on the order of 3.5 microns. It is this spacing that determines the holding voltage of the SCR 130. The width W may be of the order of 70 microns. An advantage of the invention is that it requires only a small area (i.e., approximately 5000 microns using sub-0.5 $\mu$  design rules). For example, the layout of Figure 10 results in an area of the order of 5600 microns.

A preferred layout for a vertical pnp triggered ESD protection circuit according to the invention is shown in Figure 11. The lateral npn transistors 104 are formed using n-type diffused regions 106,108 within substrate 102. The n-type diffused regions 106 and 108 alternate between connecting to ground Vss (n-type diffused regions 106) and the I/O pad 110 (n-type diffused regions 108). The spacing L2 between diffused regions 106 and 108 is preferably the minimum allowed by the design rules (i.e., of the order of 0.7 microns). Each diffusion width, D1 and D2 is of the order of 3 microns. Two diodes/vertical pnp transistors 122 are formed in well regions 118 using two p-type diffused regions 117 and one n-type diffused region 120. The p-regions 117 are connected to the I/O pad 110. The n-region 120 is connected to Vcc. The p-and n- diffused region widths D3 may be of the order of 5 microns and the spacing L1 between the p-type diffused region 117 and the nearest n-type diffused region 106 may be of the order of 3.5 microns. It is this spacing that determines the holding voltage of the SCR 130. The width W may be of the order of 70 microns.

Figure 12 illustrates a first alternative substrate biasing circuit for triggering lateral npn 104 according to the invention. In the embodiment of Figure 12, substrate biasing circuit 150 comprises a lateral PMOS transistor 162 consisting of p-type source/drain regions 154 and 156 in n-well 152 and gate 158. Source/drain region 154

is connected to pad 110 and source/ drain region 156 is connected to a p-type diffused region 160 located directly within substrate 102. The gate 158 is connected such that the PMOS transistor 162 conducts current during the ESD event. As current is conducted through the PMOS transistor 162 and to p-type diffused region 160, the voltage across substrate resistance 114 is increased. Operation then continues in the manner described above.

Lateral npn transistor 104 triggers due to the increased voltage across the substrate resistance 114, clamps the voltage at the pad 110 and dissipates the ESD current.

Figure 13 illustrates a second alternative substrate biasing circuit for triggering lateral npn 104 according to the invention. In the embodiment of Figure 12, substrate biasing circuit 150 comprises a lateral NMOS transistor 170 consisting of n-type source/drain regions 164 and 166 and gate 168. Source/drain region 164 is connected to pad 110 and source/ drain region 166 is connected to a p-type diffused region 160 located directly within substrate 102. The gate 168 is connected such that the NMOS transistor 170 conducts current during the ESD event. As current is conducted through the NMOS transistor 170 and to p-type diffused region 160, the voltage across substrate resistance 114 is increased. Operation then continues in the manner described above. Lateral npn transistor 104 triggers due to the increased voltage across the substrate resistance 114, clamps the voltage at the pad 110 and dissipates the ESD current.

While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description.

## Claims

1. An ESD protection circuit formed in a substrate comprising:

at least one lateral npn transistor for which said substrate serves as a base ; and  
a substrate biasing circuit for triggering the or each lateral npn transistor by increasing a voltage across the substrate resistance during an ESD event.

2. The ESD protection circuit of Claim 1, wherein said substrate biasing circuit comprises;

a diode including an inherent vertical pnp transistor having a collector which is connected to a base of said lateral npn transistor for triggering said lateral npn transistor through the substrate resistance.

3. The ESD protection circuit of Claim 2, wherein said diode comprises:

a p-type diffused region located within a well region and connected to an input/output pad; and  
a n-type diffused region located within said well region and connected to a supply voltage.

4. The ESD protection circuit of Claim 3, further comprising at least one inherent silicon-controlled rectifier (SCR) formed of said p-type diffused region, said well region, said substrate, and an emitter region of said lateral npn transistor.

5. The ESD protection circuit of any preceding claim, wherein said lateral npn transistor comprises an emitter connected to a ground potential and a collector connected to an input/output pad.

6. The ESD protection circuit of any Claims 2 to 5, wherein said diode comprises a Darlington string of diodes connected between an I/O pad and a supply voltage.

7. The ESD protection circuit of Claim 6, further comprising: a plurality of npn transistors each having a collector connected to said I/O pad, an emitter connected to a ground potential, and a base connected to said ground potential through an inherent resistance in said substrate.

8. The ESD protection circuit of Claim 6 or Claim 7 further comprising: a reverse diode connected in parallel with said Darlington string of diodes for leakage reduction.

9. The ESD protection circuit of any of Claims 6 to 8 further comprising: at least one resistor connected between an emitter and base of at least one diode in said Darlington string of diodes.

10. The ESD protection circuit of any of Claim 6 to 9, wherein said Darlington string of diodes comprises between 2 and 12 diodes.

11. The ESD protection circuit of any preceding claim, wherein said substrate biasing circuit comprises:

a PMOS transistor located in a well region and connected to an input/output pad; said p-type diffused region being located in the substrate and connected to the PMOS transistor.

12. The ESD protection circuit of any preceding claim, wherein said substrate biasing circuit comprises:

a NMOS transistor connected to an input/output pad; said

p-type diffused region being located in the substrate and connected to the NMOS transistor.

13. The ESD protection device of any of Claims 6 to 12, wherein

said plurality of lateral npn transistors each includes a diffused emitter region connected to a low supply voltage and a diffused collector region connected to an input/output pad, and

said plurality of pn diodes being connected in a Darlington circuit between said input/output pad and a high supply voltage.

14. The ESD protection circuit of Claim 13, wherein each of said plurality of pn diodes comprises an inherent vertical pnp transistor.

15. The ESD protection circuit of Claim 13 or Claim 14, wherein each of said plurality of pn diodes comprises:

a n-type well region located in said substrate, said n-type well region forming a base region of said inherent vertical pnp transistor;

a n-type diffused region within said n-type well region for providing a connection to said base region of said inherent vertical pnp transistor; and

a p-type diffused region within said n-type well region, said p-type diffused region forming an emitter region of said inherent vertical pnp transistor.

16. The ESD protection circuit of any of Claims 13 to 15, further comprising at least one inherent silicon-controlled rectifier (SCR) formed of said p-type diffused region and said well region of one of said plurality of pn diodes, said substrate, and a diffused emitter region of one of said plurality of lateral npn transistors.

17. The ESD protection circuit of any of Claims 13 to 16, further comprising a reverse diode connected in parallel with said plurality of pn diodes.

18. The ESD protection circuit of any of Claims 13 to 17, further comprising at least one resistor connected between said n-type diffused region and said p-type diffused region of at least one diode of said plurality of pn diodes for balancing the current in said pn diodes of said plurality of pn diodes and for increasing the clamp voltage for mixed voltage operation.

19. A method for ESD protection comprising the steps of:

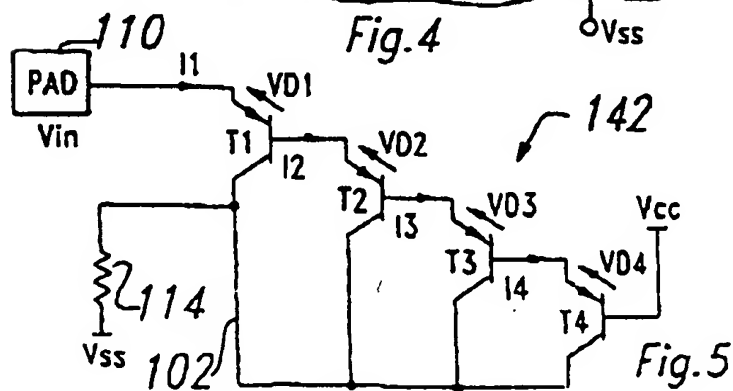
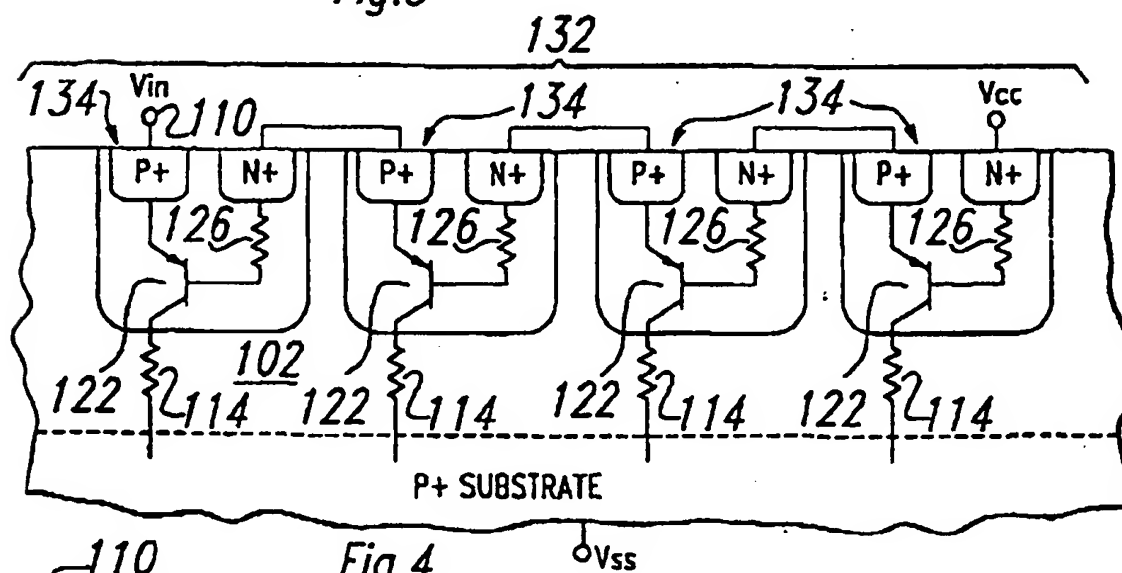
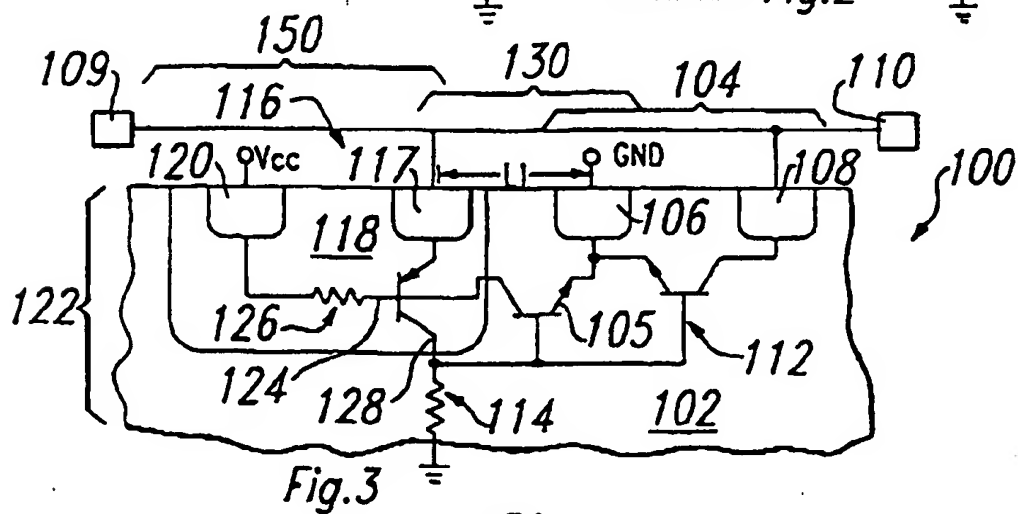
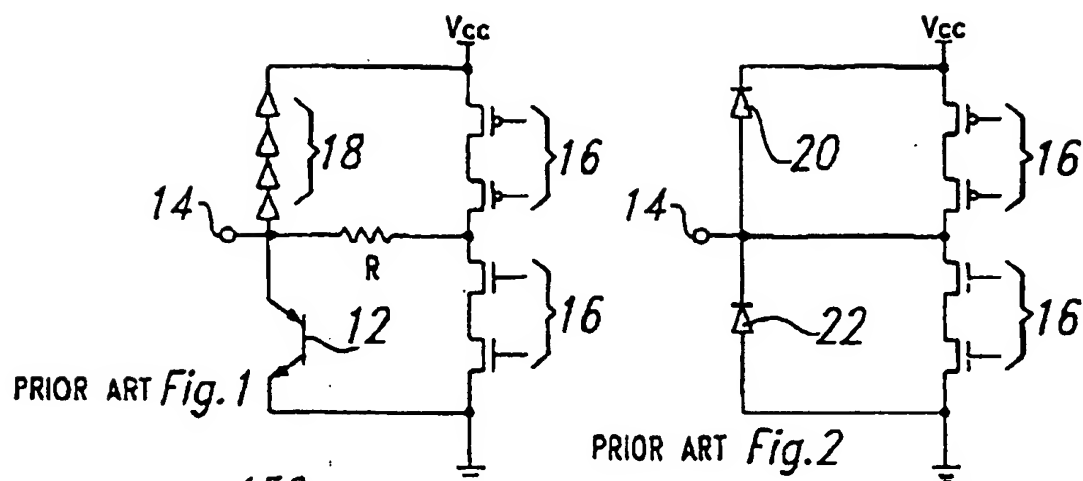
connecting at least one pn diode having an inherent vertical pnp transistor to an input/output

put pad;

connecting at least one lateral npn transistor to a low supply voltage and said input/output pad, such that a substrate forms a base of said at least one lateral npn transistor and a collector of said inherent vertical pnp transistor; conducting ESD current through said inherent vertical pnp transistor to increase a voltage level at said base of said at least one npn transistor; and triggering said at least one lateral npn transistor when said voltage level at said base of said at least one npn transistor reaches a base-emitter forward bias voltage.

20. The method of Claim 19 further comprising the step of; triggering an inherent silicon-controlled rectifier (SCR) under ESD conditions comprised of at least one pn diode and said at least one lateral npn transistor.
21. The method of Claim 20, further comprising; using said SCR to clamp a voltage level at said input/output pad of the order of 4.5 V.
22. The method of Claim 20 or Claim 21 further comprising; tuning a holding voltage of the SCR.
23. The method of any of Claims 19 to 22, further; performing said conducting ESD current step when a voltage level at said input/output pad reaches approximately 0.8 V.
24. The method of any of Claim 19 to Claim 23, further comprising; using said at least one lateral npn transistor to clamp a voltage level at said input/output pad to approximately 5-7 V.





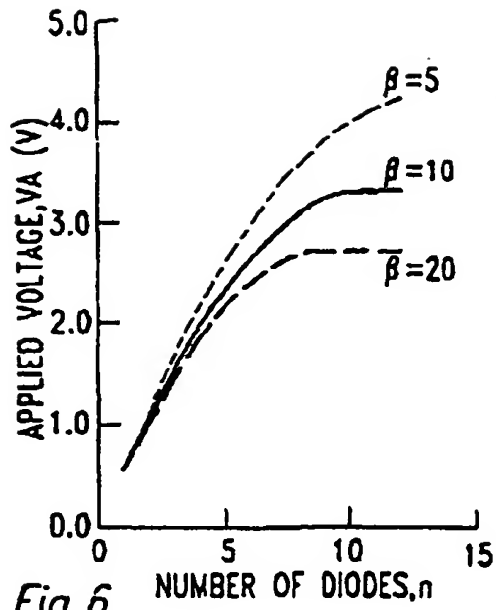


Fig. 6

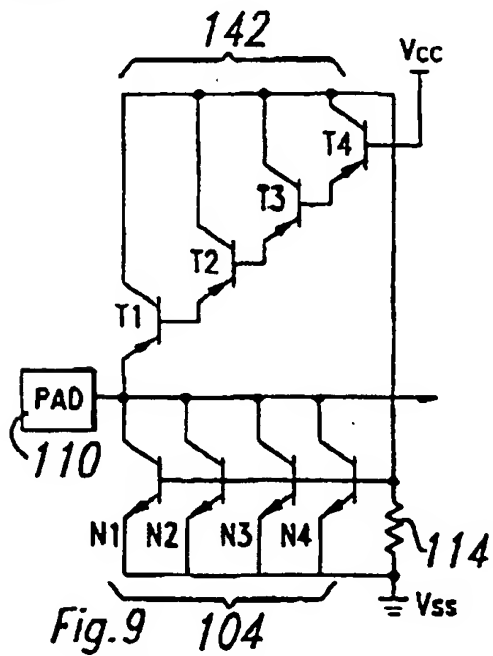


Fig. 9

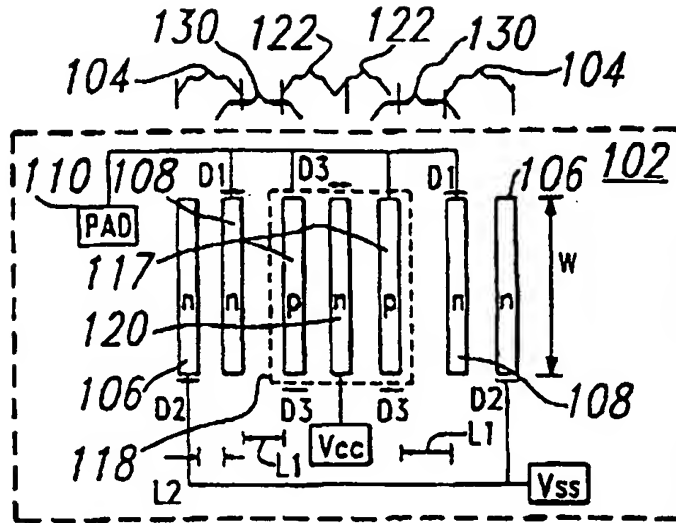


Fig. 11

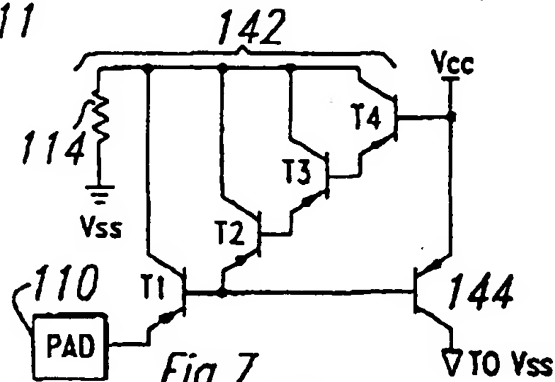


Fig. 7

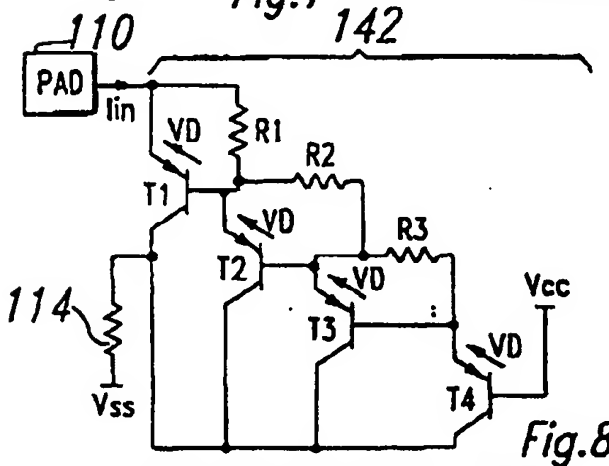


Fig. 8

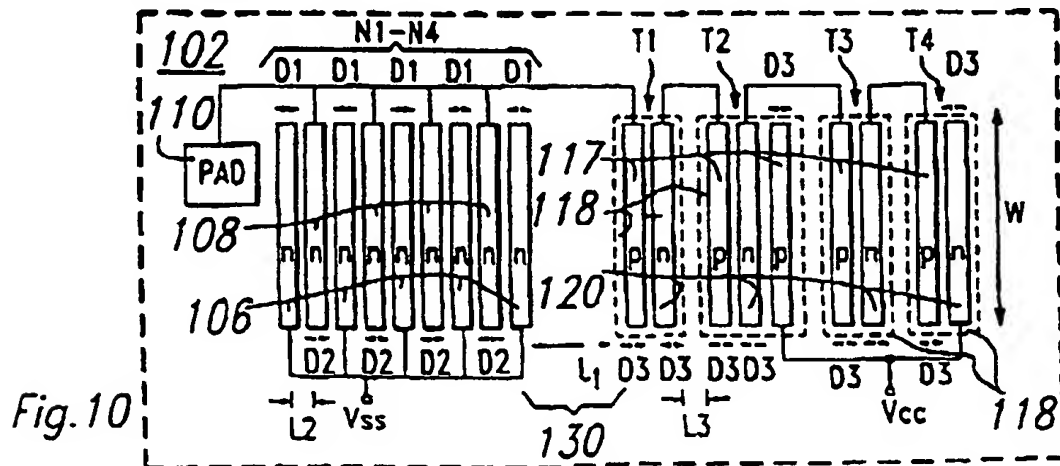
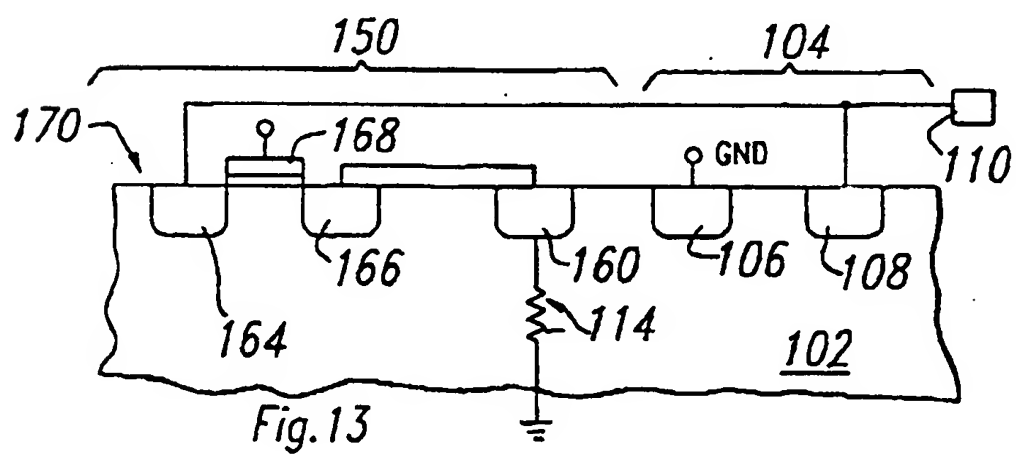
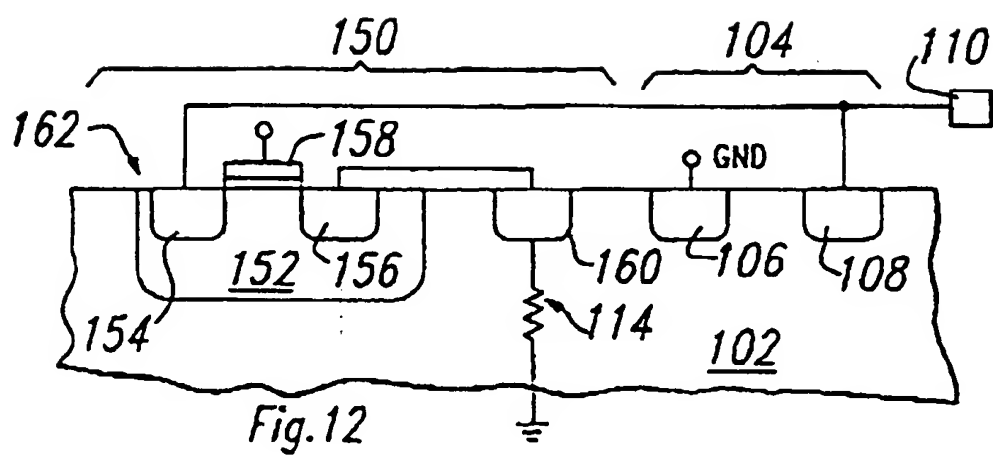


Fig. 10





European Patent  
Office

# EUROPEAN SEARCH REPORT

Application Number  
EP 96 11 1201

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	US-A-5 290 724 (LEACH JERALD G) 1 March 1994 * column 2, line 2 - line 6 * * column 6, line 63 - line 66 * * column 8, line 3 - line 64 * * column 14, line 55 - line 56; figures 6,7 *	1,5,11,12	H01L27/02
X	EP-A-0 546 698 (SGS THOMSON MICROELECTRONICS) 16 June 1993 * abstract; figures *	1,5	
A	EP-A-0 404 008 (TOKYO SHIBAURA ELECTRIC CO) 27 December 1990 * claim 6; figure 2 *	2	
A	EP-A-0 084 177 (TOKYO SHIBAURA ELECTRIC CO) 27 July 1983 * page 1, line 9 - line 11; figure 1 *	11,12	
The present search report has been drawn up for all claims			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
			H01L
Place of search		Date of completion of the search	Examiner
THE HAGUE		4 October 1996	Vendange, P
<p><b>CATEGORY OF CITED DOCUMENTS</b></p> <p>X : particularly relevant if taken alone  Y : particularly relevant if combined with another document of the same category  A : technological background  O : non-written disclosure  P : intermediate document</p> <p>T : theory or principle underlying the invention  E : earlier patent document, but published on, or after the filing date  D : document cited in the application  L : document cited for other reasons</p> <p>.....  &amp; : member of the same patent family, corresponding document</p>			

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